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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/541,857	04/03/2000	James Digby Collier	491.039US1	4161

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EXAMINER	
LAM, TUAN THIEU	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 02/22/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/541,857	Applicant(s) COLLIER ET AL.	
	Examiner Tuan T. Lam	Art Unit 2816	

-- The MAILING DATE of this communication app ars on th cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2001* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *31-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 7 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This is a response to the amendment filed 12/6/2001. The pending claims are 31-58.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 31-43, 45-56 and 58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (USP 4,356,411), prior art of record. Figure 5 of Suzuki et al. shows a frequency divider circuit (267) comprising a first signal generator (not shown) to generate a first periodic clock signal (CLOCK) to be frequency divided by the frequency divider (267), an even number of amplifier stages (2 amplifier stages 241, 242) connected in series, with an output of a last amplifier stage (242) connected to input of a first amplifier stage (241) and each amplifier each having an associated propagation delay which varies in response to a respective control signal (CLOCK), wherein the first signal generator (CLOCK) coupled to an odd amplifier (241), an even amplifier (242) is activated in anti-phase of the first periodic signal (CLOCK/), the propagation delay through the even amplifier stage (242) decreases when the propagation delay through the odd amplifier stage (241) increases, and wherein said first signal generator are arranged to generate said first periodic signal such that the propagation delay through each of the amplifier stages is modulated about half the period of said first periodic signal.

The difference seen between Suzuki et al. and the present invention is that Suzuki et al. uses a single clock signal (CLOCK) for both even and odd amplifiers instead of a clock signal

and its complementary for respective even and odd amplifiers as called for in claims 31, 48 and 58. Although Suzuki et al. uses a single clock, the even and odd amplifiers (241 and 242) are responsive to positive edges and negative edges, respectively. That is, the even and odd amplifiers (241) operate on different phases of the clock signal. One skilled in the art would have been recognized that the P-channel transistors 269, 271 receiving the CLOCK signal is equivalent to N channel transistors receiving the opposite phase of the clock signal (CLOCK). Therefore, it would have been obvious to person skilled in the art at the time of the invention was made to replace the P channel transistors 269, 271 coupled to the clock signal (CLOCK) with N channel transistors coupled to an inverter for receiving a complementary of the clock signal because the substitution is equivalent and will not alter the operation of the frequency divider.

3. Regarding claim 32, the number of amplifiers is two.

4. Regarding claim 33, Suzuki et al. shows a single frequency divider. However, it is known and obvious to one skilled in the art to cascade a plurality of Suzuki et al.'s frequency divider to obtain a desired frequency divided signal. Therefore, the limitation of cascading a plurality of frequency dividers will not be patentable under 35USC 103(a).

5. Regarding claims 34 and 49, each amplifier stage of Suzuki et al.'s figure 4 is a differential amplifier.

6. Regarding claims 35-36 and 50-51, the connection logic circuitry is seen as transistors 254, 256, the N channel transistors that replace P channel transistors 269 and 271.

7. Regarding claims 37-38 and 52-53, each amplifier stage of Suzuki et al. inherently has hysteresis characteristics which varies in response to the clock signal.

8. Regarding claims 39-42 and 54-55, each amplifier stage is CMOS.

9. Regarding claims 43 and 56, Suzuki et al. does not specifically indicate the clock signal (CLOCK) in a range of 100 Mhz. However, it is known that CMOS technology is capable of operating with frequencies of 100 Mhz or higher. Therefore, the limitation of using the clock signal at 100 Mhz is seen to be inherently presently in Suzuki et al.'s frequency dividers.

10. Regarding claim 45, first and second inverters are seen as transistors 243-244, 248, 249; 257, 258, 262, 263.

11. Regarding claim 46, N channel transistors are seen as transistors 253-256.

12. Regarding claim 47, Suzuki et al. does not disclose the size of n channel controlling transistors (253-256) is larger than the size of n channel transistors (243 and 248). However, it is notoriously well known to implement the n channel controlling transistors with a larger size in order to reset the crossed inverters (2430244, 248, 249) at a quicker speed thus preventing an erroneous operation. Therefore, the limitation of having n channel controlling transistor at a larger size than the size of the n channel inverting transistors will not be patentable under 35USC 103(a).

13. Claims 44 and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (USP 4,356,411), prior art of record, in view of Maemura (USP 5,172,400), newly cited prior art. Figure 5 of Suzuki et al. reference teaches and suggest all limitations recited in claims 31 and 48, as noted above, but fails to show logic circuitry connected in series between at least two of the amplifier stages in order to enable division by ratios other than simple powers of two as called for in claims 44 and 57. Figure 15 of Maemura reference teaches the use of a logic circuitry (41) implemented in between two amplifier stage to obtain a division ratio other than power of two. Therefore, it would have been obvious to a person skilled in the art at the time of

the invention was made to include the logic circuitry (41) of Maemura in the circuit arrangement of Suzuki et al.'s figure for the flexibility of obtaining a frequency divided output other than power of two.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. In this regard, applicant cited prior art has been carefully considered.

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 703-305-3791. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P Callahan can be reached on 703-308-4876. The fax phone numbers for

the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-3872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Tuan T. Lam
Primary Examiner
Art Unit 2816

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February 17, 2002